REMARKS

By the present amendment and response, independent claims 1, 7, 11, 12, and 15 have been amended to overcome the Examiner's objections. Claims 1-17 are pending in the present application. Reconsideration and allowance of pending claims 1-17 in view of the above amendments and the following remarks are requested.

Best Available Copy

A. Rejection of Claims 1, 2, 7, 11, 12, and 15 under 35 USC §103(a)

The Examiner has rejected claims 1, 2, 7, 11, 12, and 15 under 35 USC §103(a) as being unpatentable over "Synthesis and Simulation of Digital Systems Containing Interacting Hardware and Software Components," ACM/IEEE, 1992, pp. 225-230, by Gupta et al. (hereinafter "Gupta") in view of U.S. patent number 5,870,588 to Rompaey et al. (hereinafter "Rompaey"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1, 7, 11, 12, and 15, is patentably distinguishable over Gupta and Rompaey, singly or in any combination thereof.

The present invention, as defined by amended independent claim 1, recites, among other things, running a unified simulation of a system design and an application program as a single process in a simulation environment, where the simulation environment is a cycle accurate simulation environment, and where a programming model of a processor component communicates with a programming model of a memory component in the

PAGE 14/23 * RCVD AT 2/17/2005 5:11:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:949 282 1002 * DURATION (mm-ss):08-48

simulation environment through a transaction based interconnect. As disclosed in the present application, the present invention integrates hardware and software components of a system design in a single unified simulation environment. As disclosed in the present application, execute and update processes of a cycle based simulation provide cycle accurate information to the simulation environment, which provides enough detail to a system engineer to accurately validate the performance of a design. As disclosed in the present application, the cycle accurate simulation environment advantageously executes significantly faster than conventional event driven simulation environments.

As disclosed in the present application, in one embodiment of the present invention's cycle accurate, single unified simulation environment, a processor component of a system model communicates with a memory component of the system model through a transaction based interconnect, which includes high level general purpose programming language function calls. As disclosed in the present application, a processor component of the system model may simulate the operation of the operating system during the simulation by executing the instructions of the operating system. As a result, in the present invention, a single cycle accurate simulation environment can advantageously simulate both the hardware components (memory and processor) as well as a software component (the operating system application). Also, since the cycle accurate, unified simulation environment runs as one process, simulation time is advantageously reduced and debugging is advantageously simplified.

PAGE 15/23 * RCVD AT 2/17/2005 5:11:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729308 * CSID:949 282 1002 * DURATION (mm-ss):08-48

In contrast to the present invention as defined by amended independent claim 1, Gupta does not teach, disclose, or suggest running a unified simulation of a system design and an application program as a single process in a simulation environment, where the simulation environment is a cycle accurate simulation environment, and where a programming model of a processor component communicates with a programming model of a memory component in the simulation environment through a transaction based interconnect. Gupta specifically discloses an event-driven simulator (Poseidon) that performs concurrent simulation of multiple functional models implemented either as a program or as application-specific hardware. See, for example, Gupta, pages 228-229. As discussed above, the present invention's cycle accurate simulation environment advantageously executes significantly faster than a conventional event driven simulation environment.

Furthermore, Gupta fails to teach, disclose, or suggest a cycle accurate single simulation environment as specified in amended independent claim 1 and as defined in the present application. In Gupta, each model has an associated clock signal and clock cycle-time sued for its simulation. See, for example, Gupta, page 229. However, Gupta fails to teach, disclose, or suggest a unified simulation of a system design and an application program that runs as a single process, as specified by amended independent claim 1. Thus, the event-driven simulator disclosed in Gupta is not and cannot be a cycle accurate single simulation environment as specified in amended independent claim 1.

PAGE 16/23 * RCVD AT 2/17/2005 5:11:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729308 * CSID:949 282 1002 * DURATION (mm-ss):08-48

Also, in Gupta, a connection between two models may be either a direct connection through a wire, or a port connection through a register or queue. See, for example, page 229 of Gupta. However, Gupta fails to teach, disclose, or remotely suggest a programming model of a processor component communicating with a programming model of a memory component in the simulation environment through a transaction based interconnect, as specified in amended independent claim 1.

In contrast to the present invention as defined by amended independent claim 1, Rompaey does not teach, disclose, or suggest running a unified simulation of a system design and an application program as a single process in a simulation environment, where the simulation environment is a cycle accurate simulation environment, and where a programming model of a processor component communicates with a programming model of a memory component in the simulation environment through a transaction based interconnect. Rompaey specifically discloses a simulation of a digital system including software subsystems that are executed on one or more hardware subsystems. See, for example, Rompaey, column 6, lines 36-49. In Rompaey, the hardware subsystems comprise any one or more of processor cores, off-the-shelf components, custom components, ASICs, processors, and boards, while the software subsystems comprise machine instructions for the hardware subsystems. See, for example, Rompaey, column 6, lines 49-53.

Rompaey further discloses removing inter-process communication with remote-procedure-call semantics between a plurality of processes by "merging the plurality of

PAGE 17/23 * RCVD AT 2/17/2005 5:11:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729308 * CSID:949 282 1002 * DURATION (mm-ss):08-48

processes" (see, for example, Rompaey, column 7, lines 24-27), which is not the same as running a cycle accurate unified simulation of a system design and an application program in a single process, as specified in amended independent claim 1. In Rompaey, a "process" is a container for a number of host language encapsulations of a component. See, for example, Rompaey, column 11, lines 40-41. Thus, Rompaey fails to teach, disclose, or suggest running a cycle accurate unified simulation of a system design and an application program as a single process, as specified in amended independent claims 1.

In fact, Rompaey fails to teach, disclose, or suggest a cycle accurate, single simulation environment as specified in amended independent claim 1 and as defined in the present application. Also, Rompaey fails to teach, disclose, or suggest a programming model of a processor component communicating with a programming model of a memory component in a cycle accurate, single simulation environment through a transaction based interconnect, as specified by amended independent claim 1. Thus, Rompaey fails to cure the basic deficiencies of Gupta discussed above.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not suggested, disclosed, or taught by Gupta and Rompaey, either singly or in combination thereof. As such, the present invention, as defined by amended independent claim 1, is patentably distinguishable over Gupta and Rompaey. Thus claim 2 depending from amended independent claim 1 is, *a fortiori*, also patentably distinguishable over Gupta and

PAGE 18/23 * RCVD AT 2/17/2005 5:11:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729308 * CSID:949 282 1002 * DURATION (mm-ss):08-48

Rompaey for at least the reasons presented above and also for additional limitations contained in the dependent claim. Amended independent claims 7, 11, 12, and 15 recite similar limitations as amended independent claim 1. Thus, for similar reasons as discussed above, Applicant respectfully submits that the present invention, as defined by amended independent claims 7, 11, 12, and 15, is not suggested, disclosed, or taught by Gupta and Rompaey, either singly or in combination thereof. As such, the present invention, as defined by amended independent claims 7, 11, 12, and 15, is patentably distinguishable over Gupta and Rompaey.

B. Rejection of Claims 1-17 under 35 USC §103(a)

The Examiner has further rejected claims 1-17 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,615,357 to Loran P. Ball ("Ball") in view of Rompaey. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1, 7, 11, 12, and 15, is patentably distinguishable over Ball and Rompaey, singly or in any combination thereof.

In contrast to the present invention as defined by amended independent claim 1, Ball does not teach, disclose, or suggest running a unified simulation of a system design and an application program as a single process in a simulation environment, where the simulation environment is a cycle accurate simulation environment, and where a programming model of a processor component communicates with a programming model

PAGE 19/23 * RCVD AT 2/17/2005 5:11:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729308 * CSID:949 282 1002 * DURATION (mm-ss):08-48

of a memory component in the simulation environment through a transaction based interconnect. Ball is directed to a system and method for verifying processor performance. Ball specifically discloses a simulator that employs a benchmark program, such as benchmark program 50, to generate performance statistics. See, for example, column 9, lines 27-32 and Figure 5A of Ball. However, Ball fails to teach, disclose, or suggest a running a unified simulation of a system design and an application program as a single process, as specified in amended independent claim 1.

Ball further discloses providing trace file samples to cycle accurate model 60, which uses the information contained in the traces, in conjunction with static benchmark program 50, to generate a collection of performance statistics 62. See, for example, column 9, lines 44-49. However, as discussed above, Ball fails to teach, disclose, or suggest a unified simulation of a system design and an application program as a single process, as specified in amended independent claim 1. As such, cycle accurate model 60 is not a cycle accurate simulation environment, as specified in amended independent claim 1. Furthermore, Ball fails to teach, disclose, or suggest a cycle accurate simulation environment. Additionally, Ball fails to teach, disclose, or suggest a programming model of a processor component communicating with a programming model of a memory component in a cycle accurate simulation environment through a transaction based interconnect, as specified in amended independent claim 1.

As discussed above, in contrast to the present invention as defined by amended independent claim 1, Rompaey does not teach, disclose, or suggest running a unified

simulation of a system design and an application program as a single process in a simulation environment, where the simulation environment is a cycle accurate simulation environment, and where a programming model of a processor component communicates with a programming model of a memory component in the simulation environment through a transaction based interconnect. Thus, Rompaey fails to cure the basic deficiencies of Ball discussed above.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not suggested, disclosed, or taught by Ball and Rompaey, either singly or in combination thereof. As such, the present invention, as defined by amended independent claim 1, is patentably distinguishable over Ball and Rompaey. Thus claims 2-6 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Ball and Rompaey for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Amended independent claims 7, 11, 12, and 15 recite similar limitations as amended independent claim 1. Thus, for similar reasons as discussed above, Applicant respectfully submits that the present invention, as defined by amended independent claims 7, 11, 12, and 15, is not suggested, disclosed, or taught by Ball and Rompaey, either singly or in combination thereof. As such, the present invention, as defined by amended independent claims 7, 11, 12, and 15, is patentably distinguishable over Gupta and Rompaey. Thus, claims 8-10 depending from amended independent claim 7, claims 13-14 depending from amended independent claim 12, and claims 16-17

PAGE 21/23 * RCVD AT 2/17/2005 5:11:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729308 * CSID:949 282 1002 * DURATION (mm-ss):08-48

depending from amended independent claim 15 are, *a fortiori*, also patentably distinguishable over Ball and Rompaey for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. **Conclusion**

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 7, 11, 12, and 15, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-17 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to claims 1-17 pending in the present application is respectfully requested.

PAGE 22/23 * RCVD AT 2/17/2005 5:11:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729308 * CSID:949 282 1002 * DURATION (mm-ss):08-48

Attorney Docket No.: 02CON359P

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 2/17/05

Michael Farjami, Esq.
Reg. No. 38, 135

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

CERTIFICATE OF FACSIMILE TRANSMISSION
I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number **703-872-9306** on the date stated below. The facsimile transmission report indicated that the facsimile transmission was successful.

Date of Facsimile: 2/17/05

Christina Carter
Name of Person Performing Facsimile Transmission

Christina Carter 2/17/05
Signature Date

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: _____

_____
Name of Person Mailing Paper and/or Fee

_____
Signature Date

PAGE 23/23 * RCVD AT 2/17/2005 5:11:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:949 282 1002 * DURATION (mm-ss):08-48

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☒ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.